ABSTRACT

A turbo code encoder with an interleaver having two recursive systematic constituent code (RSC) encoders. The encoder encodes a finite sequence of informative bits without requiring a plurality of tail bits to flush the registers of each encoder to an all-zero state. The interleaver reduces the turbo code overhead by using only a single tail bit sequence. The interleaver also selectively reorders integers in accordance with a predefined set of rules.

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